AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A platform comprising:

a system memory to store output data in an isolated output area and a non-isolated area;

a memory controller hub (MCH) coupled to the system memory; and

a processor coupled to the MCH to generate a signal to the MCH, the signal indicating whether the output data is to be stored in the isolated output area or the non-isolated area, the signal generated by the processor to further cause the MCH, in response to an indication of the signal that the output data is to be stored in the isolated output area of the system memory, to receive a bus transaction indicating an isolated transaction from a graphics device to enable access to the output data stored in the isolated output area, and to transfer the output data to an isolated bit plane on the graphic device, the graphic device having the isolated bit plane for the output data from the isolated output area and a non-isolated bit plane for the output data from the non-isolated output area.

2. (Cancelled)

3. (Previously Presented) The platform of claim 1 wherein the MCH coupled between the system memory, the processor, and the graphics device, the memory control hub to permit the graphics device to access the isolated output area only when the graphics device asserts an isolated access mode.

4. (Previously Presented) The platform of claim 3 wherein the graphics device comprises:

a direct memory access (DMA) controller.

5. (Previously Presented) The platform of claim 3 wherein only the graphics device is permitted to read the isolated output area.

6. (Currently Amended) The platform of claim 1 further comprising:

an operating system (O/S) nub having a driver to write display data into the isolated output area when the processor is executing in an ~~the~~ isolated execution mode.

7. (Previously Presented) The platform of claim 3 further comprising:

a link between the graphics device and the MCH having an isolated transaction type.

8. (Original) The platform of claim 3 wherein the MCH only permits the O/S nub to write to the isolated output area.

9. (Original) The platform of claim 7 wherein the link is a secure accelerated graphics port bus.

10. (Cancelled)

11. (Previously Presented) The platform of claim 1 wherein the graphics device denies all external access to the isolated bit plane.

12. (Currently Amended) A method comprising:

establishing an isolated execution environment having an isolated execution mode by a processor generating a signal indicating whether output data is to be stored in an isolated output area or a non-isolated area of a system memory, the signal generated by the processor further causing a memory controller hub (MCH), in response to an indication of the signal that the output data is to be stored in the isolated output area of the system memory, to receive a bus transaction indicating an isolated transaction from a graphics device to enable access to the output data stored in the isolated output area, and to transfer the output data to an isolated bit plane on the graphic device, the graphic device having the isolated bit plane for the output data from the isolated output area and a non-isolated bit plane for the output data from the non-isolated output area; and

preventing access to the output data in the isolated output area of the system memory by any requester not operating in the isolated execution mode.

13. (Cancelled)

14. (Previously Presented) The method of claim 12 further comprising:

issuing an isolated direct memory access (DMA) request for display data in the isolated output area from the graphics device; and

refreshing the display based on the display data.

15. (Previously Presented) The method of claim 12 wherein preventing comprises:

identifying if an isolated attribute is present in a request for access to the isolated output area; and

denying the request if no isolated attribute is present.

16. (Currently Amended) The method of claim 12 further comprising:

loading data from the isolated output area into ~~a~~ the isolated bit plane on the graphics device; and

denying all external access to the isolated bit plane.

17. (Currently Amended) The method of claim 16 further comprising:

defining a first window on an output display to present an image corresponding to the isolated bit plane; and

occluding all windows on the display but the first window.

18. (Previously Presented) The method of claim 12 further comprising:

retrieving data from the isolated output area;

displaying an image corresponding to the data; and

occluding the image prior to a platform transitioning out of the isolated execution mode.

19. (Previously Presented) An apparatus comprising:

a processor to generate a signal to a memory controller hub (MCH), the signal indicating whether output data is to be stored in an isolated output area or a non-isolated area of a system memory, the signal generated by the processor to further cause the MCH, in response to an indication of the signal that the output data is to be stored in the isolated output area of the system memory, to receive a bus transaction indicating an isolated transaction from a graphics device to enable access to the output data stored in the isolated output area, and to transfer the output data to an isolated bit plane on the graphic device, the graphic device having the isolated bit plane for the output data from the isolated output area and a non-isolated bit plane for the output data from the non-isolated output area.

20. (Previously Presented) The apparatus of claim 19 wherein the bus transaction is issued through a secure accelerated graphics port (AGP).

21. (Previously Presented) The apparatus of claim 19 wherein the bus transaction is issued by a direct memory access (DMA) controller of the graphics device, the DMA controller to attach an isolated attribute to any isolated output area access request.

22. (Previously Presented) The apparatus of claim 19 wherein the signal generated by the processor has an isolated attribute to indicate execution in an isolated execution mode.